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Attorney's Docket No. 67,200-613

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Tsai, et al
Serial No.: 10/ 050,322
Filed: Jan. 15, 2002
For: A Bi-Layer Photoresist Dry Development and Reactive Ion Etch Method

Group Art Unit: 1756
Examiner: Nicole M. Barreca

Commissioner for Patents
Alexandria, VA 22313

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on Aug. 30, 2004 .

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate" , 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$170.00
X	other than a small entity	$340.00

Appeal Brief fee due: $ 340.00

Certificate of Mailing

I hereby certify that this correspondence is, on the date shown below, being:

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for Patents, Alexandria, VA 22313

Kathy Dixon

Dated: Oct. 28, 2004

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of □1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) □ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
□	one month	$ 110.00	$ 55.00
□	two months	$ 430.00	$215.00
□	three months	$ 980.00	$490.00
□	four months	$1,530.00	$765.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

□ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) □ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 340.00

Extension fee (if any) $_____

TOTAL FEE DUE: $ 340.00

6. FEE PAYMENT

_X_ Attached is a Credit Card Payment Form for the sum of $ 340.00

A duplicate copy of this transmittal is attached.

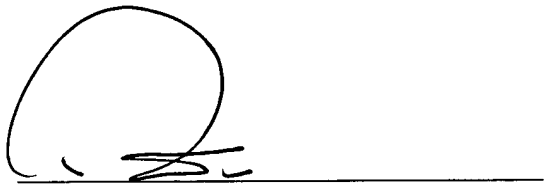
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

_X_ If any additional extension and/or fee is required, this is a request therefor to charge Visa Credit Card No. 4756 8461 9568 0263

And/Or

_X_ If any additional fee for claims is required, please charge Visa Credit Card No. 4756 8461 9568 0263



Signature of Attorney

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: Tsai et al. Group Art Unit: 1756

Serial No.: 10/050,322 Examiner: N. M. Barreca

Filed: 01/15/2002

For: A BI-LAYER PHOTORESIST DRY DEVELOPMENT AND REACTIVE ION ETCH METHOD

Attorney Docket No.: 67,200-613

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EV 435 808 505 US
Date of Deposit Oct. 28, 2004

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $340.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Mail Stop: Appeal, Commissioner for Patents, Alexandria, VA 22313-1450.

Kathy Dixon

APPEAL BRIEF

Mail Stop: Appeal
Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

APPELLANTS appeal in the captioned application from the Examiner's final rejection, dated 5/28/2004, of claims 1, 3, 5, 7, 11-13, 21-26, and 30-38.

It is urged that Examiners final rejection be reversed and that all the claims currently pending be allowed.

(1) REAL PARTY IN INTEREST

The real party in interest in the present appeal is the recorded Assignee, Taiwan Semiconductor Manufacturing Company, Ltd.

(2) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that are known to the Appellant, the Appellant's legal representative, or the assignee.

(3) STATUS OF CLAIMS

Claims 1, 3, 5, 7, 11-13, 21-26, and 30-38 are pending in the Application.

Claims 2, 4, 6, 8-10, 14-20, and 27-29 have been cancelled.

Claims 1, 3, 5, 7, 11-13, 21-26, and 30-38 stand rejected.

APPELLANTS appeal from the rejection of claims 1, 3, 5, 7, 11-13, 21-26, and 30-38.

(4) STATUS OF AMENDMENTS

A Request for Reconsideration from Final Rejection was mailed on or about 7/28/2004 including proposed amendments.

An Advisory Action was mailed on 8/24/2004 refusing entry of the proposed amendments included in the Request for Reconsideration.

A Supplemental amendment correcting claim dependency errors in claims 7 and 11 thereby overcoming rejections under 35 USC § 112, second paragraph and correcting typographical errors in claims 26 and 32 was filed on or about October 27, 2004. It is assumed supplemental amendment has been entered at the time of filing the Appeal Brief and the Claims Appendix reflects the changes in the supplemental amendment.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1, 25, and 32 are directed to a method for a method for etching an opening using a bi-layer photoresist to improve an etching resolution and reduce particulate contamination.

For example, several problems with prior art bi-layer development processes are recognized by Applicants including ashing processes as outlined in paragraph 009 where Applicants recognize the problem of residual particle contamination generated in ashing and etching processes including carry out such processes in separate chambers. Applicants disclosed and claimed invention is directed to overcome these shortcomings in the prior art.

Independent claim 1 outlines a bi-layer resist mask development process where a first (non-silicon containing) and second resist layers (silicon containing) are formed with a specified thickness followed by a patterning process for the second (upper) resist layer and a dry development process of the first resist layer (lower layer), followed by an etching process, and followed by an in-situ ashing process to remove remaining overlying resist layers.

Independent claim 25 further specifies the bi-layer development process including dry development gases, and applicable wavelengths of exposure of the second resist layer. In addition, claim 25 further outlines in-situ etching, ashing and plasma cleaning steps.

Independent claim 32 further specifies a sequence of in-situ steps following patterning the bi-layer resist including an ashing process to remove the second resist layer, followed by etching an opening, followed by removing the first resist layer by a second ashing process, followed by etching through an underlying resist layer, and followed by a plasma cleaning process.

Figures 1A to 1G show cross sectional side view representations of a portion a semiconductor device according to an exemplary **step wise** manufacturing process as embodied in the various claims. Figure 3 shows an exemplary process flow as embodied in the various claims. Paragraphs 0033 to 0044 outline exemplary process steps with respect to Figures 1A to 1G. Paragraph 0046 outlines the benefits and problems overcome by Applicants disclosed and claimed invention

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3, 5, 7, 11-13, 21, 23-26, and 30-38 stand rejected under 35 USC 102(e) as being anticipated by Ohuchi (US Patent 6,576,562).

2. Claim 22 stands rejected under 35 USC 103(a) as being unpatentable over Ohuchi and further in view of Smith (US Patent 6,388,226).

(8) ARGUMENT

Rejection under 35 USC 102(e)

Claims 1, 3, 5, 7, 11, 21, 25, 32, and 36-38

Ohuchi discloses a method for forming an etched opening in a substrate using a mask material including a carbon content of 80%

or more (see Abstract). The relevant part of the teachings of Ohuchi in etching an opening into a substrate using a bi-layer methodology is outlined in Figures 7A through 7F and at columns 29-31 (see col 29, lines 13-20). Ohuchi discloses and teaches a method for forming a dual damascene opening using a bi-layer mask forming methodology.

Ohuchi critically teaches the use of a lower **organic** layer film (in contrast with Applicants first resist layer) that has an **aromatic ring** and **carbon content** of **80 wt%** or more, preferably more than 90 wt% (see col 29, lines 31-35) to provide a high etching resistance. Applicants, by contrast claim a first resist layer. Ohuchi teaches that a conventional resist layer has a carbon content of about 70 wt % (col 30, lines 38-39). Thus the teachings of Ohuchi in this respect alone, are insufficient to anticipate Applicants disclosed and claimed invention; rather, the disclosure of Ohuchi directly teaches away from Applicants disclosed and claimed invention by teaching using an aromatic ring containing **organic layer** with a carbon content of greater than about 80 %.

Applicants further claim "providing a silicon containing photoresist layer over the first resist layer to form a second

resist layer thinner than the first resist layer". Significantly, Ohuchi does not disclose any particular thicknesses of the first resist or the silicon containing second resist layer for forming a damascene opening as shown in Figures 7A-7F in the bi-layer embodiment, discussed in columns 29 to 31, which is the relevant portion applicable to Applicants disclosed and claimed invention.

Ohuchi does teach, however, that the lower organic layer having a carbon content of greater than 80 wt %, disclosed to be a critical part Ohuchi's invention, may be **thinner** than a conventional resist film due to its superior etching resistance from, thus teaching that it is thinner than the uppermost (second resist layer) (see col 30, lines 37-40; col 31, lines 4-12). Thus, Ohuchi, in this respect alone, is also insufficient to anticipate Applicants disclosed and claimed invention, but rather teaches directly away therefrom.

The disclosure of Ohuchi is clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claims 1, 12, 25, 26, and 32

Further, with respect to claims 1, 25, and 32 and with respect to claims 12 and 26, following patterning the upper

resist layer, Ohuchi teaches that in transferring the pattern (opening) in the first resist layer to the lower organic layer (e.g., Applicants first resist layer), that the overlying mask (patterned resist layers) may be left in place, maintaining a substantially constant thickness following etching of the via opening, thereby teaching away from removal of the lower organic layer (Applicants first resist layer) prior to forming the wiring (trench line) groove over the via opening (col 30, lines 52-63). Thus, Ohuchi teaches that the resist layers are left in place following etching of the via opening to "suppress deterioration of the dielectric insulating film" (col 30, lines 55-65).

In contrast, Applicants in claim 1 claim "carrying out an in-situ ashing process to remove remaining overlying resist layers comprising the first and second resist layers" following etching of an opening into the substrate.

Thus, Ohuchi does not teach carrying out an ashing process to remove overlying resist layers comprising the first and second resist layers following formation of an opening as disclosed and claimed by Applicants in claim 1, but rather teaches directly away therefrom. Moreover, Ohuchi does not teach or suggest "removing the second resist layer according to a first ashing

process prior to the second plasma etching process" as claimed by Applicants in claim 12; or "carrying out an in-situ oxygen ashing process to remove overlying resist layers comprising at least the first resist layer" as claimed by Applicants in claim 25; or "wherein the second resist layer is removed in-situ according to a first oxygen ashing process prior to the step of etching" as claimed by Applicants in claim 25; or the sequence of steps as claimed by Applicants in claim 32:

"carrying out a first in-situ oxygen ashing process to remove the second resist layer;

plasma etching in-situ an opening in the dielectric insulating layer;

carrying out a second in-situ oxygen ashing process to remove the first resist layer;"

Moreover, Ohuchi does not disclose or suggest that the etching and ashing processes are carried out in-situ.

The disclosure of Ohuchi is clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claims 13, 25, 32, 33, and 35

Further with respect to claims 25 and 32, and with respect to claim 13, 33 and 35, Ohuchi does not suggest or disclose a

plasma cleaning process as claimed by Applicants in claims 13, 25, 32, and 35 following formation of the opening or a plasma cleaning process following etching through a bottom etch stop layer as claimed by Applicants in claims 25, 32, 33, and 35.

The disclosure of Ohuchi is clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claims 23, 30, 34

As mentioned above with respect to the first resist layer, Ohuchi specifically teaches away from using a conventional photoresist in the first resist layer and further, nowhere suggests or discloses Applicants disclosed and claimed first resist materials as claimed in claims 23, 30, and 34.

The disclosure of Ohuchi is clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claims 24 and 31

Ohuchi nowhere discloses that the silicon in the upper second resist layer comprises silicon incorporated from a silylation process.

Ohuchi is clearly insufficient to anticipate or make obvious Applicants disclosed and claimed invention.

Rejection under 35 USC 103(a)

Claim 22

Applicants reiterate the comments made above with respect to claim 1, and submit that neither Ohuchi nor Smith, alone or in combination, suggest or disclose Applicants disclosed and claimed invention, or recognize the problem, or provide a solution to the problem that Applicants solved by their disclosed and claimed invention.

"A method for etching an opening using a bi-layer photoresist to improve an etching resolution and reduce particulate contamination".

CONCLUSION

Examiner has not met the burden of establishing anticipation by Ohuchi of Applicants claimed invention. Moreover, Examiner has not met the burden of establishing a *prima facie* case of obviousness. Rather, APPELLANTS disclosed and claimed invention has been demonstrated to be nonobvious. None of the cited

references, individually or in combination, recognize or solve the problem recognized and solved by Applicants.

The fact that Examiner can produce no references, alone or in combination, disclosing or suggesting APPELLANTS disclosed and claimed invention strongly supports a conclusion of patentability.

It is therefore respectfully submitted that Examiners final rejection of Appellants claims is improper under the statutory standard of 35 USC § 102(e) and/or 35 USC § 103(a) as interpreted by both the Board and the Courts.

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Tung & Associates

By: _____

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CLAIMS APPENDIX

1. A method for etching an opening using a bi-layer photoresist to improve an etching resolution and reduce particulate contamination comprising the steps of:

providing an unpatterned non-silicon containing organic resinous layer over a substrate to form a first resist layer;

providing a silicon containing photoresist layer over the first resist layer to form a second resist layer thinner than the first resist layer;

exposing the second resist layer to form a second resist layer pattern revealing first resist layer portions;

dry developing said first resist layer portions according to the second resist layer pattern to reveal the substrate according to a first plasma etching process comprising nitrogen and oxygen to form an etching mask;

plasma etching according to a second plasma etching process an opening into the substrate according to the etching mask; and,

carrying out an in-situ ashing process to remove remaining overlying resist layers comprising the first and second resist layers.

2. (cancelled)

3. The method of claim 1, wherein the first resist layer comprises a non-photoactive polymer.

4. (cancelled)

5. The method of claim 1, wherein the activating light source comprises a wavelength selected from the group consisting of about 157 nanometers and about 193 nanometers.

6. (cancelled)

7. The method of claim 1, wherein the first resist layer has a thickness of about 1000 Angstroms to about 5000 Angstroms and the second resist layer has a thickness of about 500 Angstroms to about 3000 Angstroms.

8. - 10. (cancelled)

11. The method of claim 1, wherein the semiconductor feature is selected from the group consisting of a via hole, a trench line, and a contact hole.

12. The method of claim 1, further comprising the step of removing the second resist layer according to a first ashing process prior to the second plasma etching process.

13. The method of claim 1, wherein the in-situ ashing process comprises an oxygen containing plasma and a component selected from the group consisting of nitrogen and fluorine to simultaneously clean plasma reactor contact surfaces.

14. - 20. (cancelled)

21. The method of claim 1, wherein the dry development plasma is formed of plasma forming gases consisting essentially of nitrogen and oxygen.

22. The method of claim 1, wherein the dry development plasma is formed of plasma forming gases consisting essentially of nitrogen, oxygen, and argon.

23. The method of claim 1, wherein the first resist layer is selected from the group consisting of an I-line photoresist, an acrylic polymer, and a polyvinyl alcohol polymer.

24. The method of claim 1, wherein the second resist layer comprises a DUV photoresist wherein the silicon comprises silicon incorporated from one of a silylation process and from silicon monomers included in the photoresist.

25. A method for etching a semiconductor device feature using a bi-layer photoresist to improve an opening etching resolution and reduce particulate contamination comprising the steps of:

providing a non-silicon containing photoresist layer over a dielectric insulating layer to from a first resist layer;

providing a silicon containing photoresist layer over the first resist layer to form a second resist layer thinner than the first resist layer;

patterning the second resist layer according to a photolithographic exposure process comprising a wavelength selected from the group consisting of 157 nm and 193 nm;

wet developing the second resist layer to form a patterned second resist layer;

dry etching the first resist layer according to a dry etching chemistry formed by supplying gases consisting essentially of nitrogen, oxygen, and optionally, argon, to reveal the dielectric insulating layer to form an etching mask;

plasma etching in-situ an opening in the dielectric

insulating layer according to the etching mask;

carrying out an in-situ oxygen ashing process to remove overlying resist layers comprising at least the first resist layer; and,

carrying out an in-situ plasma cleaning process comprising a component selected from the group consisting of fluorine and nitrogen to clean plasma reactor contact surfaces.

26. The method of claim 25, wherein the second resist layer is removed in-situ according to a first oxygen ashing process prior to the step of etching.

27. - 29. (cancelled)

30. The method of claim 25, wherein the first resist layer is selected from the group consisting of an I-line photoresist, an acrylic polymer, and a polyvinyl alcohol polymer.

31. The method of claim 25, wherein the second resist layer comprises a DUV photoresist wherein the silicon comprises silicon incorporated from one of a silylation process and from silicon monomers contained within the photoresist.

32. (currently amended) A method for etching a semiconductor device feature using a bi-layer photoresist to improve an opening etching resolution and reduce particulate contamination comprising the steps of:

providing a non-silicon containing photoresist layer over a dielectric insulating layer to ~~from~~ form a first resist layer;

providing a silicon containing photoresist layer over the first resist layer to form a second resist layer thinner than the first resist layer;

patterning the second resist layer according to a photolithographic exposure process comprising a wavelength selected from the group consisting of 157 nm and 193 nm;

wet developing the second resist layer to form a patterned second resist layer;

dry etching the first resist layer according to a dry etching chemistry comprising nitrogen, oxygen, and argon, to reveal the dielectric insulating layer to form an etching mask;

carrying out a first in-situ oxygen ashing process to remove the second resist layer;

plasma etching in-situ an opening in the dielectric insulating layer;

carrying out a second in-situ oxygen ashing process to remove the first resist layer;

plasma etching in-situ through a bottom etch stop layer comprising the substrate; and,

carrying out an in-situ plasma cleaning process comprising a component selected from the group consisting of fluorine and nitrogen to clean plasma reactor contact surfaces.

33. The method of claim 32, wherein the first and second in-situ ashing processes comprise adding a component selected from the group consisting of fluorine and nitrogen to simultaneously clean plasma contact surfaces.

34. The method of claim 32, wherein the first resist layer is selected from the group consisting of an I-line photoresist, an acrylic polymer, and a polyvinyl alcohol polymer.

35. The method of claim 1, further comprising the steps of:

etching through a bottom etch stop layer comprising the substrate; and,

carrying out an in-situ plasma cleaning process comprising a component selected from the group consisting of fluorine and nitrogen to clean plasma reactor contact surfaces.

36. The method of claim 1, wherein the first and second plasma etching processes and the ashing process are carried out in a dual source RF power plasma reactor comprising an RF biasing power source.

37. The method of claim 25, wherein the plasma reactor comprises a dual source RF power plasma reactor comprising an RF biasing power source.

38. The method of claim 32, wherein the plasma reactor comprises a dual source RF power plasma reactor comprising an RF biasing power source.

EVIDENCE APPENDIX

None.

Related Proceedings Appendix

None.